NORFOLK STATE UNIVERSITY

FACULTY OF ENGINEERING

DEPARTMENT OF ELECTRONIC ENGINEERING

A PROJECT REPORT ON

INVERTER, 2-INPUT NAND AND NOR GATES DESIGN USING LTSPICE AND ELECTRIC

BY

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APRIL 2023

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## Project Overview

Logic gates are fundamental building blocks of digital electronics and are essential for designing and building complex digital systems. They perform logical operations on binary signals (0 or 1) and produce an output based on the input signals. The importance of logic gates can be understood by their following applications:

1. Digital circuits: Logic gates are used to design digital circuits that are used in a wide range of applications, including computers, smartphones, televisions, and other electronic devices. These circuits can perform various operations, such as arithmetic, memory, control, and signal processing.
2. Communication systems: Logic gates are used in communication systems to encode, decode, and transmit digital signals. They are used in various communication technologies, such as telecommunication networks, wireless communication systems, and satellite communication systems.

VLSI (Very Large-Scale Integration) technology is widely used for designing and implementing logic gates. VLSI technology involves the integration of thousands to millions of transistors on a single chip, allowing for the creation of complex digital systems. In this report, some selected logic gates are designed using the Electric software EDA tool and the LTSPICE simulator.

## Project Objectives

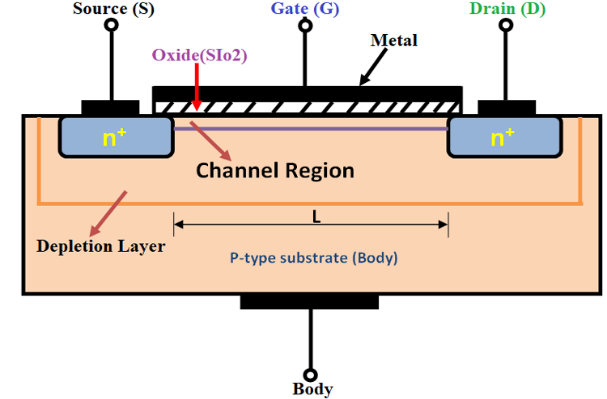
The objectives of this project is design and simulate the operation of the following gates using the Electric and LTSPICE simulator

* Design an inverter CMOS gate using the Electric layout and schematic tools
* Design 2-input NAND gate using the Electric layout and schematic tools
* Design NOR gate using the Electric layout and schematic tools

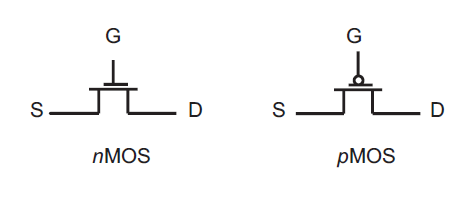
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## Operation of AND, NOR, and Inverter Gates

Generally, these gates and more which are used in almost all digital integrated systems are designed using transistors. More specifically the Metal oxide Field Effect transistors(MOSFETs) are used to design these circuits to operate according to a desired output. In the operation of a MOSFET, just like any other transistor, It needs an input voltage mostly regarded as the Gate voltage which causes creates a capacitance through a charged plate of the gate metal. From Figure 1, this charged capacitance attracts the minority carriers of the type of substrate and creates an inversion layer that actually forms the channel causing electrons to flow from one n+ side to another n+ as shown in Figure 1. There are two types of MOSFETs based on the channel formed(P channel MOSFET called PMOS and N channel MOSFET called the NMOS). This is shown in Figure 2.2. Many MOSFETs are combined to form the Complimentary Metal Oxide Semiconductor(popupoCMOS). In VLSI, a CMOS is used to form the basic logic fundamentals. The understanding basic logic fundamentals can be better understood from Table 2. 1



****Figure 2.1 Typical Diagram of MOSFET****



****Figure 2.2 Schematic Drawing of NMOS and PMOS****

Table 2.1 Truth Table for NAND Gate

|  |  |  |
| --- | --- | --- |
| INPUT(A) | INPUT B | NAND OUTPUT() |
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

Table 2.2 Truth Table for NOR Gate

|  |  |  |
| --- | --- | --- |
| INPUT(A) | INPUT B | NOR OUTPUT() |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

Table 2.3 Truth Table for Inverter

|  |  |
| --- | --- |
| INPUT(A) | OUTPUT() |
| 0 | 1 |
| 1 | 0 |

It should be understood that, the 0s and 1s we normally use is a conventional representation of the actual input or output voltages. The input voltage represents the voltage above the threshold voltage of the channel for which the MOSFET will be in the ‘’on’’ state. Contrary, the MOSFET is regarded to be in the off state when the gate voltage is less than the threshold voltage. In this work a zero represents a 0V whiles a one represents a 5V.

### Parts of the MOSFET

As observed in Figure 2.2 the end node denoted by the letter D is called the drain whiles the S is called the source. Generally, depending on the type of MOSFETS, holes or electrons are moved from the source to the drain. In the case of an NMOS, electrons move from the source to the drain and hence conventional direction of current(drain current) is from the drain to the source. In the case of a PMOS, holes move from the source to the drain and hence current is expected to travel in the same direction as the holes. The gate is denoted by G. The source is always connected to ground for an NMOS whiles the drain is connected to the ground for a PMOS. Another node called the VDD is connected to the drain for an NMOS and Source for a PMOS. The VDD serves as the output voltage across whatever load is connected to the MOSFETs. Operating as a switch, the MOSFET will only have an output of 1 when the MOSFETs is in the “ON” state and the VDD is connected across the load. Likewise, the output is 0 when the MOSFET does not operate and hence the ground voltage(0V) is connected to the load. This is illustrated in Figure 2.2. Thus the light will only turn “ON” when the gate voltage is greater than the threshold voltage and vice versa when the gate voltage is 0V.

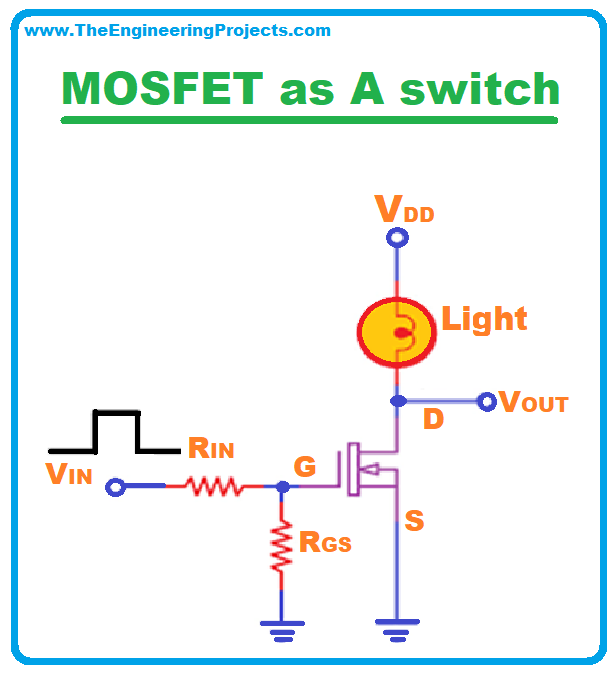


Figure 2.3 Operation of NMOS

Likewise the opposite fashion can be described for a PMOS. In a P-channel device, the conventional flow of drain current is in the negative direction so a negative gate-source voltage is applied to switch the transistor “ON”. This is achieved because the P-channel MOSFET is “upside down” with its source terminal tied to the positive supply +VDD. Then when the switch goes LOW, the MOSFET turns “ON” and when the switch goes HIGH the MOSFET turns “OFF”.

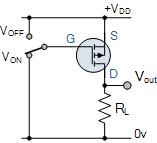


Figure 2.4 PMOS Operation

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## Simulation of Inverter

### Schematic Simulation

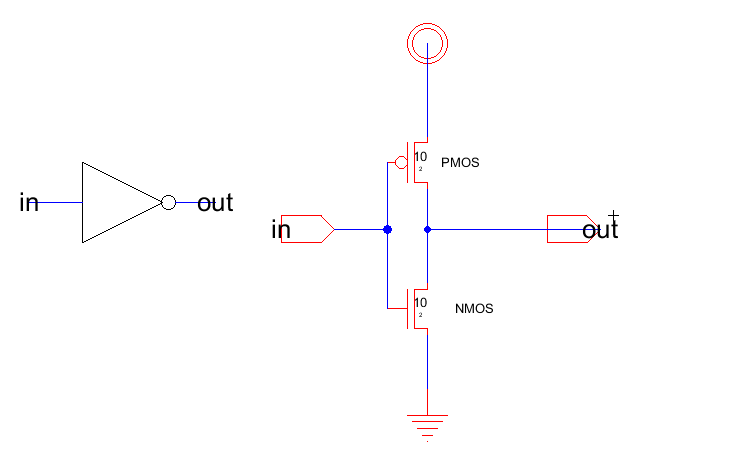
From this truth table, it is evident that a combination of NMOS and PMOS can give the required output expected from an inverter. Thus the two circuits can switch interchangeably to give the opposite output. The schematic drawing is shown in Figure 3.1 . In the schematics simulation, the circuit was first drawn with inputs parameters; width and length of the channel. An icon was then created to represent the conventional sign of an Inverter.

Figure 3.1 Schematics of Inverter

### Layout Simulation

The layout simulation captures all connections of the inverter using N and P-active wells, PMOS and NMOS modules metal-polysilicon nodes metal connections for the output. The Layout is shown in Figure 3.2 below

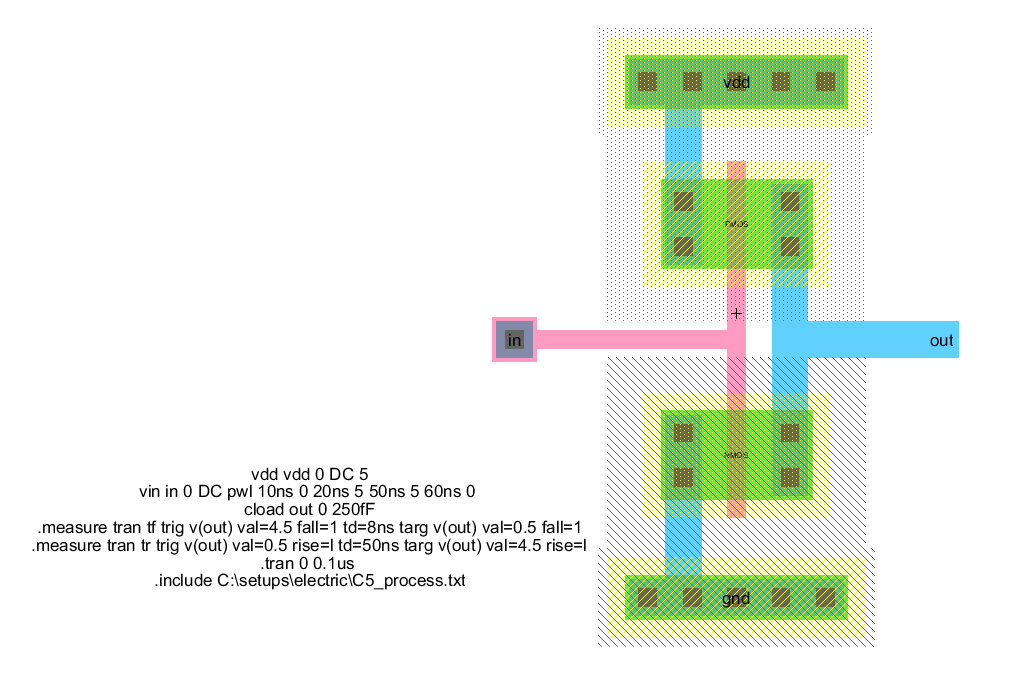


Figure 3.2 Layout of Inverter

A set of codes were input in the SPICE code editor and sweep DC analysis simulation was conducted for both schematic and layout views The same codes were used to evaluate their waveforms output. The input and output waveforms were were then compare to the Inverter truth table. The same waveform of input and output signals were observed for both the schematic and layout drawing. The paramters used are shown in Table 3.4 whiles the results is shown in Figure 3.3.

Table 3.1 Inverter Parameters

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| VDD | PWM signal | Gate Size for PMOS | | Gate Size for NMOS | |
| 5V | Vmax= 5V =digital 1 | L | W | L | W |
|  | Vmin= 0V= digital 0 | 2 | 10 | 2 | 10 |

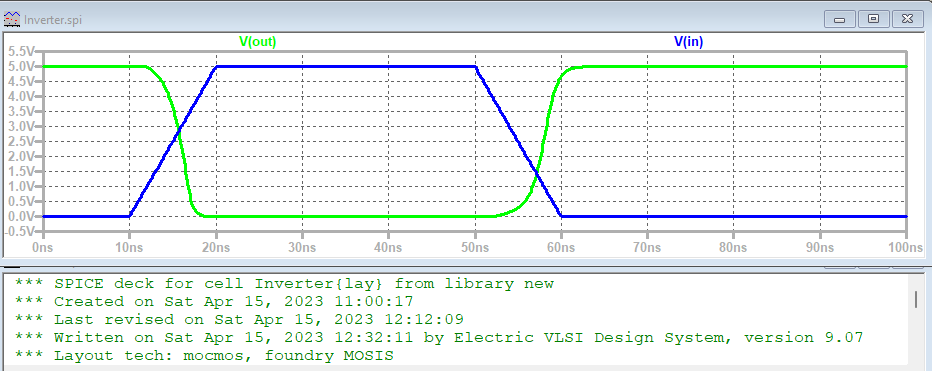


Figure 3.3 Waveform Results of Inverter Input and Output

It could be observed that rise and fall times of the input and out signals are the same. The time delays are also the same for both signals. As the output delays in the 0V, the input is also delayed in the 5V. This depicts the behavior of an inverter. Thus the input is always inverted as described in the truth table in Table 2.3

## Simulation of 2-Input NAND Gate

For the NAND the same parameters used for the Inverter were loaded. The only change was with the input pulse signals, which was generally based on arbitrary values. Using random delay periods between 0V and 5V to create a PWM signal. Figure 3.4 shows the schematic design

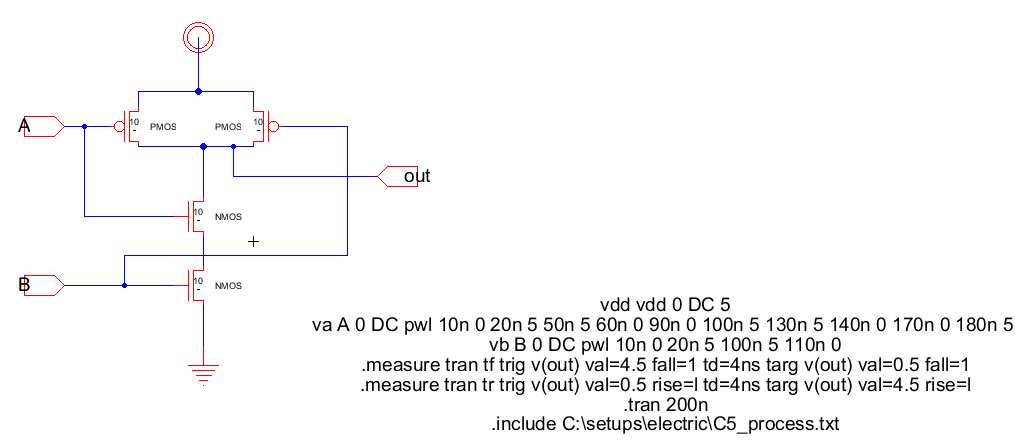
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Figure 3.4 NAND Schematic Design

Figure 3.5 and 3.6 shows the layout design and the input-output waveforms.

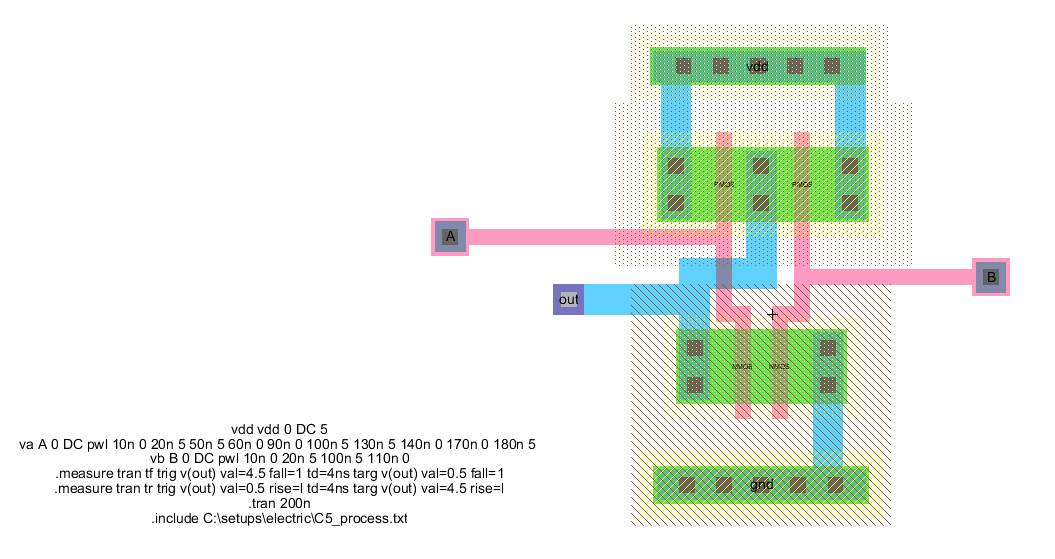


Figure 3.5 2-Input NAND Layout Design

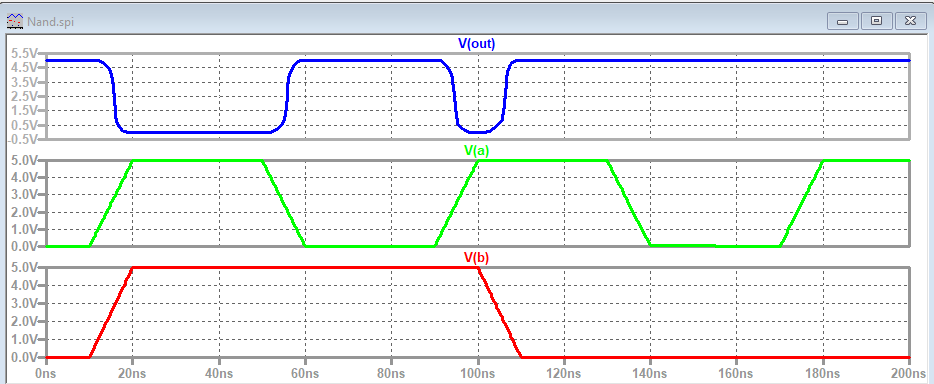


Figure 3.6 Input-Output Waveform of 2-Input NAND Gate

Table 3.3 describes the signal waveform in details

Table 3.2 Analysis of 2-Input NAND Signal Waveforms

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Time(ns) | Input V(a) | Digital Representation | Input V(b) | Digital Representation | Output(Vout) | Digital Representation |
| 20ns-50ns | 5V | 1 | 5V | 1 | 0V | 0 |
| 60ns-90ns | 0V | 0 | 5V | 1 | 5V | 1 |
| 110ns-200ns | 5V | 1 | 0V | 0 | 5V | 1 |

## 2-Input NOR Gate Simulation

For the NOR gate, the same parameters used for the 2-Input NAND gate were loaded. The only change was with the input pulse signals, which was generally based on arbitrary values. Using random delay periods between 0V and 5V to create a PWM signal. Figure 3.7 shows the schematic design.

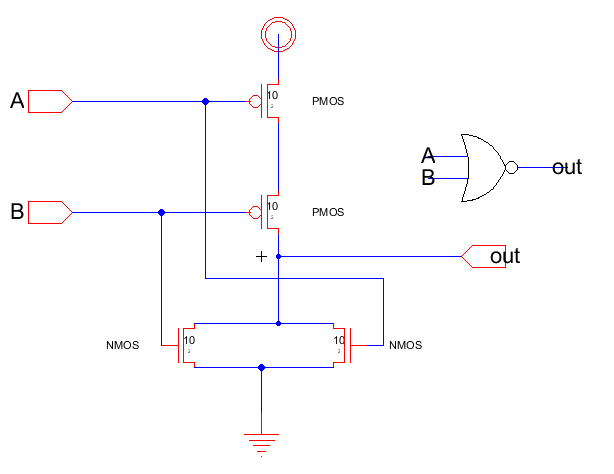


Figure 3.7 2-Input NOR Gate Schematic Design

Figure 3.8 and 3.9 shows the layout design and the input-output waveforms respectively.

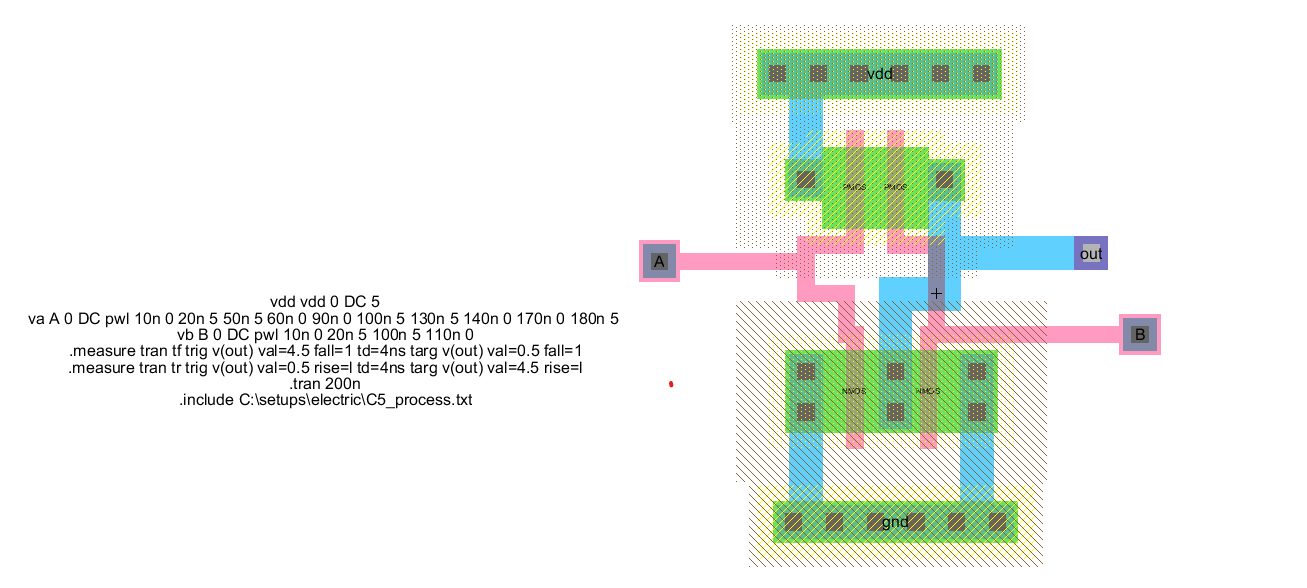


Figure 3.8 2-Input NOR Gate Layout Design

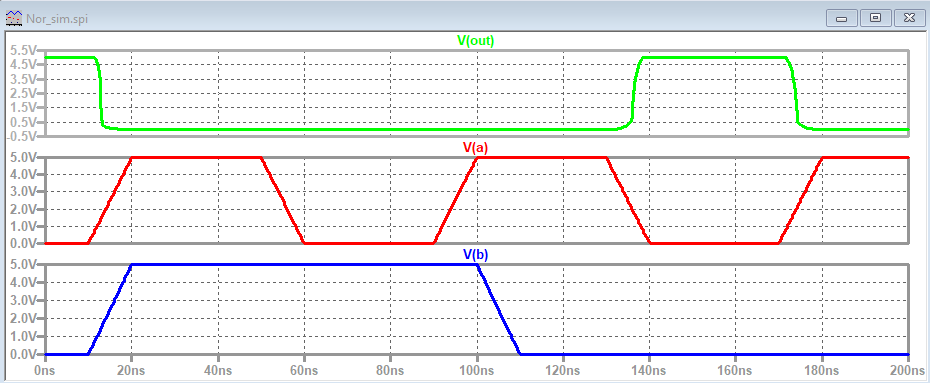


Figure 3.9 Input-Output Waveform of 2-Input NOR Gate

Table 3.4 describes the signal waveform in detail. It could be observed that the digital representation of the voltage matches the truth table of a NOR gate described in Table 2.2

Table 3.3 Analysis of 2-Input NOR Signal Waveforms

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Time(ns) | Input V(a) | Digital Representation | Input V(b) | Digital Representation | Output(Vout) | Digital Representation |
| 20ns-50ns | 5V | 1 | 5V | 1 | 0V | 0 |
| 60ns-90ns | 0V | 0 | 5V | 1 | 0V | 0 |
| 140ns-170ns | 0V | 0 | 0V | 0 | 5V | 1 |